Q1): put True or Fou1 in front of the following sentences:— [12 mark]

1- In the voltage control of single phase inverter using single pulse width modulation, the average output voltage is depend on the modulation index $M$.

2- In the voltage control of single phase inverter using multiple pulse width modulation, the number of pulse per half cycle is depend on the carrier frequency.

3- In the voltage control of single phase inverter using sinusoidal pulse width modulation, the rms output voltage is increase when the modulation index $M$ is decrease.

4- In the voltage control of single phase inverter using modified sinusoidal pulse width modulation, we cannot obtain modulation index $M$ greater than unity.

Q2): Chose the correct answer:— [12 mark]

1- In the step down DC to DC converter the average output voltage is increase, if the duty cycle is .......... (increase, decrease, kept constant)

2- For a three phase full wave diode rectifier with resistive load, the average output voltage is .................

$\frac{3\sqrt{3}V_m}{2\pi}$, $\frac{3V_m}{2\pi}$, $\frac{3\sqrt{3}V_m}{\pi}$, $\frac{2\sqrt{3}V_m}{2\pi}$

3- In the DC to AC converter with an input voltage of 12 volt and with output frequency of 50 Hz, the average output voltage is .............. when the load is high inductive load.

(14.24 volt, 8.5 volt, 5.8 volt, 0.00 volt)

4- The peak inverse voltage across any Thyristor in the Single phase full wave rectifier is ...............volt

(Vm, $-V_m$, $2V_m$, $-2V_m$)
Q3): A- Draw the following circuits clearly:-

1- Three phase half wave controlled rectifier with inductive load
2- Three phase inverter with star connected high inductive load
3- Single phase full wave controlled rectifier

B- Give four applications for industrial electronic in the daily life

Q4): For the step down converter with R-L load, if the battery voltage is 200 volt, load resistance is 8 ohm, load inductance is 12mH, the chopping frequency is 2kHz, the duty cycle is 50% and with neglect back e.m.f., draw the circuit diagram of the converter and then Calculate:

1- The minimum instantaneous load current.
2- The maximum instantaneous inductor current.
3- The maximum peak to peak resistance current.
4- The average value of the load current.
5- The rms load current.
6- The effective input resistance seen by the source.
7- The rms battery current.

Q5): For the single phase full bridge uncontrolled Rectifier, the supply voltage is 220 volt with frequency of 50 Hz, if the load is a high Inductive load, draw the circuit diagram of the rectifier clearly and then :

a) Sketch
1- The output voltage, output current and the output power
2- The input current and the input power
3- The current wave form of the diode D₁

b) Calculate
1- The average output voltage
2- The rms output voltage
3- The average input and output power

With my best wishes
Q1: A rectangular waveguide has dimensions of (5 X 2.5 Cm). The Magnetic field component in the Z-direction is given as:

\[ H_z = C \cos \left( \frac{2\pi}{2.5} y \right) \]

Find:
1- Cutoff frequency.
2- Guided wavelength inside W.G at a frequency of 7 GHz.

Q2: The microwave network shown below has two ideal directional couplers and unknown 2-port device. The matched bolometers (1, 2, 3, and 4) have readings of 2mw, 4mw, 0.5mw and 1mw respectively.

Determine:
- (Z_1) as a function of (Z_o).
- Power supplied by source and its VSWR.

![Microwave Network Diagram]

Q3: Explain briefly the function and operation of the following microwave components:

Isolator, Variable Attenuator, Coaxial to Waveguide Adaptor.
Q4: A two-cavity klystron amplifier has the following parameters:

\[ V_0 = 1000 \text{ V} \quad R_o = 40 \text{ k}\Omega \quad I_o = 25 \text{ mA} \quad f = 3 \text{ GHz} \]
\[ D = 1\text{ mm} \quad L = 4 \text{ cm} \quad R_{sh} = 30 \text{ k}\Omega \]

\( a \)- Find the input gap voltage to give maximum voltage \( V_2 \).

\( b \)- Find the voltage gain.

\( c \)- Find the efficiency.

Q5: For the M.W circuit shown below, if the circulator is ideal, find:

\( a \)- The power reflected \((P_r)\) to the source.

\( b \)- Repeat the solution if the direction of rotation is reversed.

---

**Good Luck**
Q1 What is the throughput of a system that use pure ALOHA protocol to transmit 2000 bit frame on shared channel of 8Mbps if all stations together produce:
   a. 2000 frames per second.
   b. 3000 frames per second.
   c. Repeat (a) and (b) if the system use Slotted ALOHA protocol instead of pure ALOHA.
   [10 marks]

Q2
   A. Draw the flow diagram for the CSMA/CD protocol.
   [5 marks]
   B. List all the layers of TCP/IP protocol suite and mention their equivalent layers in the OSI model.
   [5 marks]

Q3
   A. List all the advantages and disadvantages of fiber cable.
   [6 marks]
   B. Compare between the serial and parallel transmission.
   [4 marks]

Q4
   A. List three layers of OSI layer model and list four responsibilities for each layer.
   [6 marks]
   B. List four network devices so that each two of them work in different layer, explain briefly the function of each device and mention the layer in which each device work.
   [4 marks]

Q5
   A. Given the IP address 139.188.13.241 with default subnet mask find:
      i. Number of usable IP addresses.
      ii. Network address.
      iii. Network broadcast.
      iv. First and last usable IP addresses.
      v. Repeat i, ii, iii and iv if subnet mask is change to 255.255.255.240.
      [5 marks]
   B. List the four generations of Ethernet and mention all the common implementations for each of them.
      [5 marks]
Q6 Choose the most suitable answer:

1. In .......... protocol the sender can send only one frame and wait until it receive confirmation from the receiver and then it send the next frame.
   a) Go-Back-N ARQ  b) Stop-and-wait  c) Simplest  d) none of them.

2. In wireless LAN the .......... problem occurs when three stations A, B and C are available, station C is outside the transmission range of station A, station C is outside the transmission range of station A and both stations A and C is inside the transmission range of station B.
   a. Hidden station  b. Exposed station  c. none of the pervious

3. In some frames, the source and destination addresses are .......... 
   a. unicast  b. multicast  c. broadcast  d. any one of them.

4. The .......... protocol allows a host to discover its physical address when it only knows its Internet address.
   a. ARP  b. RARP  c. FTP  d. ICMP

5. A station with .......... mobility can move from one BSS to another BSS, but the movement is confined inside one ESS.
   a. No-transition  b. BSS transition  c. ESS transition

6. In standard Ethernet the maximum length of the frame has restriction(s) which is(are) .......... 
   a. preventing one station from monopolizing the share media. 
   b. the memory used in buffer was too expensive. 
   c. Both of (a) and (b).  d. none of the pervious

7. One of the beneficial .......... features of IEEE .......... MAC protocol is the ability to establish priorities among the station in the LAN.
   a. 802.3  b. 802.5  c. 802.11  d. none of the pervious

8. The value of vulnerable time in CSMA is not depends on .......... 
   a. Frame time  b. Propagation time  c. Both of them

9. Ground propagation compare to sky propagation allow for greater distance with the .......... output power of the transmitter.
   a. Same  b. higher  c. lower

10. One of the features of .......... protocol that it used special frame to assign the ‘right to transmit data’ on the LAN.
    a. CSMA/CA  b. Token ring  c. Slotted ALOHA  d. CSMA/CA

[10 marks]
Q1: Answer three of the following:
1- Compare between linear and digital integrated circuits, give an example for each.
2- Classify integrated circuit according to its complexity, how we can overcome this complexity in the design stage.
3- What are the two types of MOS RAM, compare between them.
4- Draw a layout structure for CMOS inverter and for Schottkey transistor.

Q2: For the two input NAND gate shown in fig(1), assume $\min \beta = 30$, $V_{C_{ess}}=0.2v$, standard load current of 0.7 mA, and $V_D=0.7v$.
   (i) find the output voltage when at least one input is at low,
   (ii) determine the fan-out of the gate.

Q3: The MOS circuit shown in fig(2) is used as a voltage divider which biased from constant current source of $50 \mu A$, given $\mu_{n}C_{ox}=2.5\times10^{-5}A/V^2$, $\mu_{p}C_{ox}=1.25\times10^{-5}A/V^2$, and $V_{TN}=1v$, and $V_{TP}=-1v$. Calculate the required $W/L$ for both devices.

Q4: A CMOS inverter biased from $V_{DD}=5v$ loaded by $2pF$ capacitor and switched at frequency 100kHz. Its voltage transfer characteristic is shown in fig(3). Given $(W/L)_n=2$, $(W/L)_p=4$, $\mu_{n}C_{ox}=2\mu_{p}C_{ox}=20\mu A/V^2$.
   Calculate:
   (i) the noise margins,
   (ii) the gate power dissipation,
   (iii) rise and fall time.

Q5: A TTL NAND gate with passive pull-up resistor of 4KOhm is biased from 5 volt supply and drives 10 gates, the driven gates can be represented by 0.5pF each. Given $V_{C_{ess}}=0.2V$, $V_D=0.7V$, $R_d(diode)=30$ Ohm, and transistor $R_{C_{ess}}=20$ Ohm. Calculate the 50% propagation delay low to high and high to low times.
   If the passive resistor is replaced by active (Totem-pole) of 130 Ohm limiter, transistor and diode, Calculate the new propagation delays. What is the advantage of using the Totem-pole load.
Q1: A) Convert the two-port parameters \( Z \) to \( H \) parameters.
B) Find the short circuit admittance parameters \( Y_{11} \) and \( Y_{21} \) for the network shown in the figure.

![Network Diagram](image)

(12 Marks)

Q2: Formulate the state equations of the network shown in the Figure in the form \( \dot{X} = AX + Bu \). Apply the backward Euler formula to the time domain solution for only 2 iterations. Let the initial condition be zero. The step size \( h = 0.1 \), the source is a unit step, \( R_1 = R_2 = 1 \Omega \), \( C_1 = C_2 = 0.1 \mu F \), \( L = 0.1 \mu H \).

![Network Diagram](image)

(12 Marks)

Q3: A) Use the Newton – Raphson method to determine the positive root of the equation \( 7 \sin(x) e^{-x} = 1 \) starting from \( x_0 = 0.3 \).
B) Use the golden section search method to find the maximum of a function \( F(x) = 140 e^{-x/9} \sin(x) \) for \( 0 \leq x \leq \pi \).

(12 Marks)
Q4: Derive the transfer function of the network shown in the figure. Find the transfer function with respect to amplifier. Select \(C_1 = C_2 = 1 \text{f} \), \(A = 2\), \(G_1 = G_2 = G_3 = 1 \text{mho}\), Find the pole sensitivity with respect to amplifier.

(12Mark)

\[\text{Diagram of the network}\]

Q5: A) Write down the flow chart illustrating the Genetic Algorithm process and define each process briefly.

B) Explain with suitable example how Genetic Algorithm can be used in electronic circuit design.

(12Mark)
FPGA & MICRO Lab

Q1) Implement the following function \( f(x_3,x_2,x_1,x_0)=(0,3,7,12,15) \) (using implementation schematic xc4000) (3 mark)
Q2) Write VHDL code of system shown in figure below (the program must include A, B, C, X1, X2, X3, Z). (3 mark)

![VHDL Circuit Diagram](image)

Q3) Write program that shows the following status. without using look up table. And direct solution. Using delay 1 sec. (4 mark)

<table>
<thead>
<tr>
<th>DS3</th>
<th>DS4</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>9</td>
</tr>
</tbody>
</table>
Digital Communication Lab

Q4) The logical circuit which is used as 90 degree phase shifter in carrier synchronous block of PSK detection is:

a) NAND gate b) NOR gate c) XOR gate d) AND gate

Q5) What is the logical circuit which is used to divide the frequency of Voltage Controlled Oscillator VCO by 2 to produce VCD signal in carrier synchronous block of PSK detection? Draw the circuit?

Q6) What are the significant parameters which must be taken in to account to choose the frequencies of Frequency shift keying system.

Q7) The optimum sampling frequency for the signal in below, which satisfy the Nyquist rate:

\[ y = \sin (\pi \times 9.6 \times 10^3 t) \]

a) \[ f_s = 4.8 \times 10^3 \text{ Hz} \]

b) \[ f_s = 19.2 \times 10^3 \text{ Hz} \]

c) \[ f_s = 10.8 \times 10^3 \text{ Hz} \]

d) \[ f_s = 9.2 \times 10^3 \text{ Hz} \]
Microwave Lab

Q6) A- For the following SWR Pattern, find the reflection coefficient of the load and $\lambda g$.

B- Draw the SWR pattern for a matched load, comment on that pattern.
Machine Lab

Q9) The open-circuit characteristic of separately excited DC generator driven at 1000 r.p.m as follow:

<table>
<thead>
<tr>
<th>Field current</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1</th>
<th>1.2</th>
<th>1.4</th>
<th>1.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>O.C voltage</td>
<td>30</td>
<td>55</td>
<td>75</td>
<td>90</td>
<td>100</td>
<td>110</td>
<td>115</td>
<td>120</td>
</tr>
</tbody>
</table>

The machine has filed resistance of 100 Ω find:
  a) Open circuit voltage and exciting current
  b) The critical resistance
  c) The critical speed
Q10) A 5KVA 200/1000V, 50Hz, single phase transformer gave the following test results:

<table>
<thead>
<tr>
<th>Test Type</th>
<th>Voltage</th>
<th>Current</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>O.C (L.V side)</td>
<td>200V</td>
<td>1.2A</td>
<td>190W</td>
</tr>
<tr>
<td>S.C (H.V side)</td>
<td>50V</td>
<td>5A</td>
<td>110W</td>
</tr>
</tbody>
</table>

Calculate the parameters of the equivalent circuit.
Control Lab

Q11) Explain the work of magnetic brake in Feedback experiment.

Q12) In digital control experiments Explain how you can know the direction of the speed.

Q13) In digital control experiments Explain the effect of increasing the rate of change of the input signal on the error signal.
Power Electronic Lab

Q14) draw the equivalent circuit for UJT transistor and
Q15) PUT:

Q16) Explain how the SCR turn off?

Q17) For the table below:

<table>
<thead>
<tr>
<th>VGS (V)</th>
<th>1</th>
<th>0</th>
<th>-0.5</th>
<th>-1</th>
<th>-1.5</th>
<th>-1.7</th>
<th>-2</th>
<th>-3</th>
<th>-5</th>
<th>-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID (mA)</td>
<td>13.3</td>
<td>4.5</td>
<td>3.07</td>
<td>1.8</td>
<td>0.85</td>
<td>0.54</td>
<td>0.2</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ \begin{align*}
V_g &= \text{----------------------} \\
I_{dss} &= \text{----------------------}.
\end{align*} \]

\[ \begin{align*}
\text{What is the type of the transistor?} \\
1. \text{ Sketch the characteristic curve of PUT.}
\end{align*} \]
Q1: [15 marks]
A- In 8051 microcontroller, it is required to generate the following periodical signals on P1.0 & P1.1 respectively.

![Diagram of signals](image)

Draw the required circuit diagram and write the program for that.

B- Draw the circuit diagram required to interface 8051 microcontroller to 1K byte RAM of starting address 400H.

Q2: [15 marks]
A- Write the required instructions for 8051 microcontroller to switch from register bank 0 to register bank 2.

B- FSK-modulated binary data is received via pin T1 of timer1 of the microcontroller 8051. It is required to retransmit the demodulated binary data on P2.1 assuming the modulating frequency 1KHz for binary zero and 2KHz for binary one. Write the required assembly programs for that. Hint: use timer0 to specify a period of time (e.g. 5ms) after which timer1 is to be tested, and use timer 1 as counter.

Q3: [15 marks]
A- Compare between GDT & LDT according to:
1- Maximum size.
2- Maximum number of entries.
3- Number of the GDT or LDT table in the computer system at any instant.
4- Selectors that can be used to search through the table.
5- The name of the register that points to the starting address of the table.

B- Write a program to test the memory of a computer of size 16 Kbyte. This program fills a specific value in the whole memory and then reads it. Try 00, FFH, 55H, AAH as the specific value. Use string instructions.

Q4: [15 marks]
A- What are the addressing modes of 80386 microprocessor? Give an example on each mode.

B- State the data access protection rules for the 80386 microprocessor.